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		Application Number	09/888,838
		Filing Date	June 25, 2001
		First Named Inventor	V. Alves et al.
		Group Art Unit	2403-2132
Examiner Name	Unknown B. Lanier		
SHEET 1 OF 1	Docket Number	MORPH1160	

U.S. PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code ² (if known)			
BL	1.	US-2002/108063		Kurdahi et al.	08-08-2002	

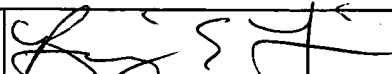
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FOREIGN PATENT DOCUMENTS								
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OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS			
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BL	2.	NOTIFICATION OF TRANSMITTAL OF INTERNATIONAL SEARCH REPORT and INTERNATIONAL SEARCH REPORT for PCT/US02/20238, dated 12/12/02, 3 pg.	
BL	3.	HAUSER, J.R. et al., "Garp: A MIPS Processor with a Reconfigurable Coprocessor," Field-Programmable Custom Computing Machines, 1997, 5th Annual IEEE Symposium in Napa Valley, CA April 16-18 1997, IEEE Comput. Soc., April 16, 1997, pages 12-21	
BL	4.	3GPP TASK FORCE, "Specification of the 3GPP Confidentiality and Integrity Algorithms - Document 2 Kasumi Specification", Version 1.0, Retrieved from the internet <URL: http://www.etsi.org/dynandca/3Gpp/3Gppconditions.html >, pages 8-20	
BL	5.	HAYNES, S.D., et al., "Configurable Multiplier Blocks for Embedding in FPGAs," Electronic Letters, IEEE Stevenage, GB, Vol. 34, No. 7, April 2, 1998, pages 638-639	

Examiner Signature		Date Considered	2/14/05
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